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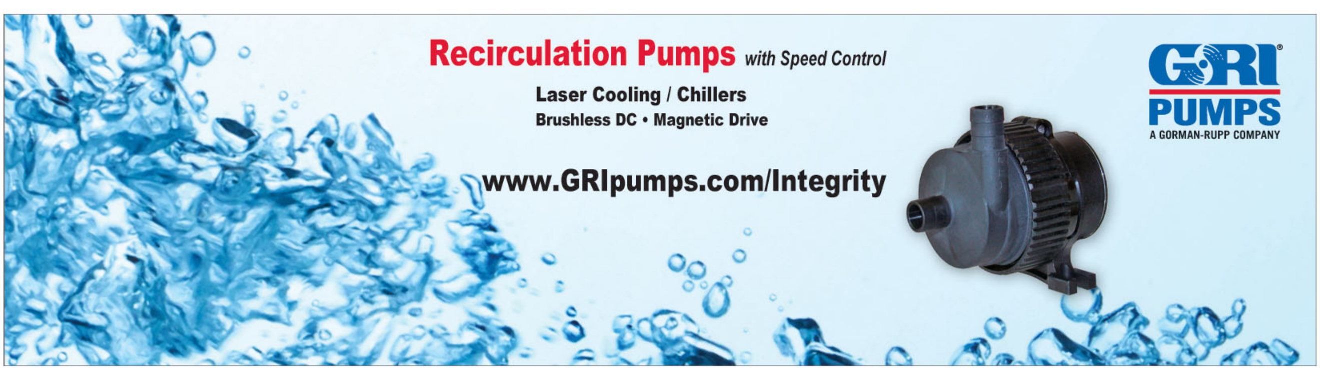

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Toward a low-voltage multiferroic transistor: Magnetic (Ga,Mn)As under ferroelectric control

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The persistent field effect control of ferromagnetism in a diluted magnetic semiconductor by low-voltage polarizing pulses is demonstrated in a ferroelectric gate field effect transistor configuration. The Curie temperature of the (Ga,Mn)As channel is unambiguously signaled by a cusp in the temperature derivative of resistance. Polarization reversal in the ferroelectric copolymer polyvinylidene fluoride with trifluoroethylene P(VDF-TrFE) by voltage pulses of less than 10 V results in a reproducible nonvolatile shift in the cusp by as much as 7%–9%. The unique combination of a relatively large spontaneous polarization and low dielectric constant of the P(VDF-TrFE) gate promises a further reduction in the operation voltage. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3076107]

Nonlinear active elements such as field effect transistors (FETs), which are central to current information technology, are based on gate voltage control of electric currents. The rapidly developing field of spintronics and its interface with conventional electronics demands that a similar control can be applied to the spin state of mobile electrons. Substantial progress in this direction has already been reported. In particular there are a number of reports of electric-field control of the Curie temperature (T_C) and magnetic anisotropy of diluted magnetic semiconductors (DMSs) in a FET device.[1–3] A qualitatively supplementary level of functionality, permitting power-down retention and adding a memory role, can be achieved by replacing the conventional gate in these devices with a nonvolatile ferroelectric gate. Recently such a nonvolatile control of the magnetic channel has been demonstrated on a hybrid system based on a thin DMS layer with integrated ferroelectric polymer gate.[4] In addition to the persistent control of ferromagnetism in the channel, this device opens opportunities for engineering ferromagnetic patterns by rewritable nanoscale control of ferroelectric domains in the gate.

The DMS used in the present work consists of a thin layer of Mn-doped GaAs in which the Mn–Mn exchange is mediated by holes in the valence band. The holes in the layer are contributed by the same Mn^{2+} ions in which the ordered magnetic moments reside, but a control of the hole density as achieved in an FET configuration alters that exchange and thus T_C. In order to achieve sufficient exchange coupling to drive a ferromagnetic transition, the Mn concentration needs to exceed 1%, with the maximum T_C of 185 K realized by present technology and requiring a substantial manganese concentration of approximately 8%.[5]

Although both conventional FET and ferroelectric gate FET (FeFET) structures on DMS have been demonstrated in principle, the currently reported structures require inconveniently large control voltages. A FeFET has a further attraction here, for the poling voltage scales with the film thickness, so it can be reduced by growing a thinner gate without impacting on the level of control. The present paper describes such structure with a well-behaved ferroelectric gate that can be poled repeatedly with less than 10 V.

The DMS channel in our ferroelectric FET was a 7 nm film of 6% Mn-doped GaAs grown by low-temperature molecular beam epitaxy as has been reported earlier.[4] Superconducting quantum interference device measurements confirmed the film as ferromagnetic at low temperature. Hall bars were defined by photolithography and wet chemical etching on the thin (Ga,Mn)As film. Electrical contact was made with electron-beam evaporated Ti/Au (15/125). The growth of a ferroelectric gate on this DMS is constrained by its sensitivity to elevated temperatures, for the Mn ions become mobile at temperatures far below the 500–600 °C required to grow ferroelectric perovskite films. Thus a 60 nm ferroelectric gate consisting of a copolymer polyvinylidene fluoride with trifluoroethylene P(VDF-TrFE) was deposited by spin coating from a 1.25% methyl ethyl ketone solution. The film was annealed at 130 °C and a 100 nm thick gold gate electrode was deposited by thermal evaporation. Polarization hysteresis loops (Fig. 1) show that the present ferroelectric FET has a gate switching voltage a factor of three smaller than in our initial proof-of-concept study,[4] exactly as expected according to the thickness scaling factor. The outlook and strategies for further reduction toward thinner films and 5 V switching are discussed below.

We have explored the impact of the polarization reversal on the magnetic properties of the channel by analyzing the transport properties in a wide temperature range. Prior to the transport measurements the conducting (Ga,Mn)As channel was prepared by switching the gate into the depletion (accumulation) state by +9.5 (−9.5) V/100 ms voltage pulses. After switching and during the transport measurements the gate was grounded in order to avoid any influence on the

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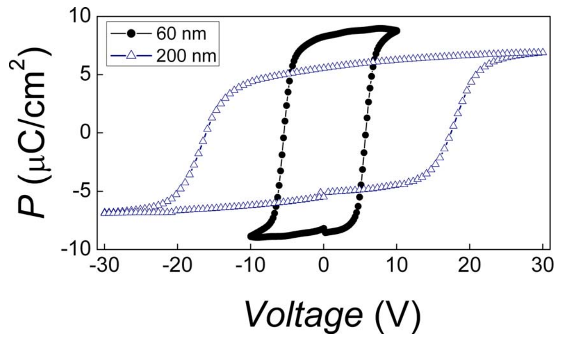

FIG. 1. (Color online) Polarization hysteresis loops of the ferroelectric gate driven by a 1 kHz triangle pulse. The 60 nm ferroelectric gate used in the present study (circles) shows a threefold reduction in the coercive voltage compared to the 180 nm gate used in the earlier study (triangles).

ferroelectric FET properties by the static charge that may accumulate on the floating gate. The gate leakage current was negligible and did not influence the measurements.

The resistance of the (Ga,Mn)As channel seen in Fig. 2 shows a weak negative temperature coefficient above the Curie temperature, characteristic of metallic conduction in the presence of weak localization. A reduction of spin-disorder scattering in the ferromagnetic state leads to a resistance peak near T_C.[6] The Hall bar with the gate poled in depletion (accumulation) shows a sheet resistance $R_\square$ of 15.6 kΩ (14.6 kΩ) at room temperature, 24.0 kΩ (20.8 kΩ) at the maximum, and 22.9 kΩ (19.4 kΩ) at 40 K. This persistent change in the channel resistance by 7% at room temperature, 15% around the peak, and 18% at 40 K and the corresponding modulation of the hole density is known to provoke a significant shift in T_C.[7] An indication that a shift has occurred in the channel is the shift in temperature of the $R_\square$ maximum between the accumulation and depletion states. This shift by 6–7 K is clearly seen in the inset of Fig. 2, with higher T_C corresponding to the accumulation state as expected.

As discussed many years ago[8] the Curie temperature in a ferromagnetic conductor with comparable carrier and fluctuating magnetic moment densities is signaled not by a maximum in the resistance $R(T)$ but rather by a cusp in its derivative dR/dT. That behavior has been convincingly demonstrated in (Ga,Mn)As.[9] Thus in Fig. 3 the derivative is plotted versus temperature, and a clear cusp is seen at 56.2 K (60.0 K) in the depletion (accumulation) state, a shift of 3.8 K. A similar shift has also been tracked in the anomalous Hall resistance, applying an Arrott-plot analysis as outlined previously.[4]

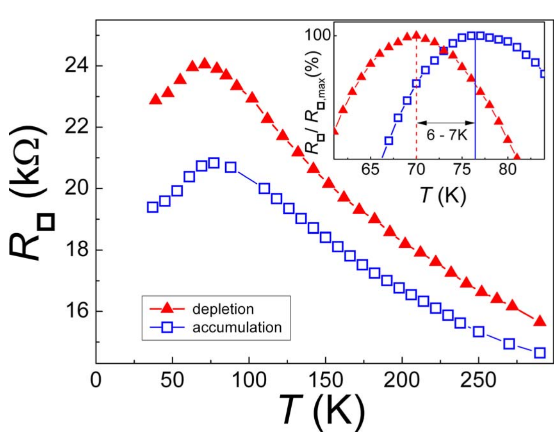

FIG. 2. (Color online) Ferroelectric gate operation and temperature dependent sheet resistance of the channel in the depletion- and accumulation-poled states. The hysteretic polarization reversal in the gate allows for nonvolatile switching of the sheet resistance. Inset: curves of resistance vs temperature normalized and zoomed in the region around the maximum occurring close to T_C. In the depletion state the maximum shifts toward lower temperatures.

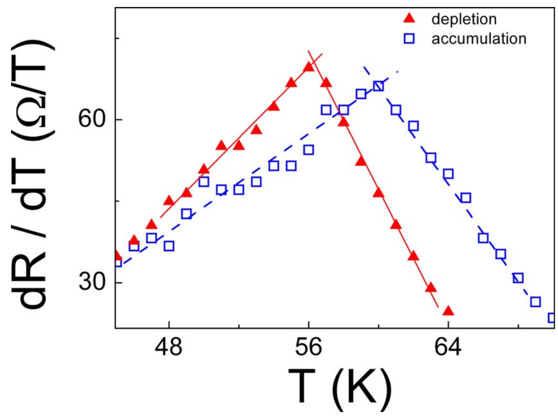

FIG. 3. (Color online) Temperature derivative of the measured resistivity for the accumulation and depletion states. The Curie temperature is very clearly signaled by cusp of the resistance derivative dR/dT. In the depletion state the position of the cusp shifts toward lower temperatures as expected.

A comparison of the present results with our previous study[4] reveals a substantial threefold reduction in the required switching voltage, directly scaling with the threefold reduction in the ferroelectric film thickness, whereas the magnitude of the T_C shift remains unchanged. This reflects an essential advantage of the ferroelectric gate, where the spontaneous polarization is thickness-independent above the size-effect thickness limit. Below this limit the spontaneous polarization degrades due to depolarization originating in the passive dielectric layer, which always exists at the ferroelectric film interface.[10] One of the significant factors determining this critical thickness is the ratio between the dielectric constants of the ferroelectric material and passive layer.[11] A larger dielectric constant of the ferroelectric material normally results in a more pronounced depolarization effect. From this point of view a unique combination of the relatively large spontaneous polarization of 7–8 $\mu C/cm^2$ and small dielectric constant of about 14 puts PVDF films in a very favorable situation, for a weak size effect permits an aggressive thickness downscaling. This agrees with recent reports showing that the critical thickness of PVDF films where a degradation of polarization starts playing a role is about 20–30 nm,[12] a factor of two or three smaller than that used in the present study. In principle, such thin ferroelectric gate layers can be switched by voltage below 5 V, making the ferroelectric gate operation compatible with standard transistor-transistor logic (TTL) circuitry. The major technical issue is to grow and anneal to quasicrystallinity ultrathin PVDF layers with sufficient electrical strength to support the poling voltage without a breakdown failure.

The relatively small effect on the T_C due to the induced hole concentration reported here is consistent with expectations for low compensation (Ga,Mn)As. In the simplest Zener model $T_C \sim xp^{1/3}$, with hole concentration p and Mn doping level x. The same weak dependence is obtained in more sophisticated models and experimentally.[13,14] However it is expected that T_C drops to zero at a finite critical hole concentration, with a precipitous decrease as the critical concentration is approached.[13] Such a drop has been reported in 7% Mn films in which the hole density was controlled by H passivation.[15] This suggests that even 100% T_C switching can be expected using the present techniques for GaMnAs materials with hole concentrations close to this critical value.

Besides ferroelectric T_C, the magnetic anisotropy energy in (Ga,Mn)As films is dependant on the hole concentration. Very recently it has been demonstrated that the anisotropy energy shows a strong dependence on p even when there are only modest changes in the Curie temperature.[3,16]

In summary we have demonstrated a magnetoelectric multiferroic device in which the Curie temperature in a DMS is controlled by low-voltage switching of a ferroelectric gate. The nonvolatile control is signaled by a clear cusp in the temperature derivative of resistance, which shows a shift of nearly 4 K between the accumulation and depletion states of the gate's polarization. Switching has been achieved with a voltage pulse of less than 10 V, and we have argued that there is no fundamental bar to lowering the switching voltage by at least a factor of three, for which further processing developments will be required. Additionally, parallel developments increasing T_C will probably be required for such FeFETs to have technological impact. The strong promise of compatibility with the standard 5 V TTL circuitry makes this hybrid multiferroic system an attractive candidate for spintronics devices, especially those requiring nonvolatile operation.

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